



VLSI Architectures for Modern Error-Correcting Codes

Xinmiao Zhang

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Error-correcting codes are ubiquitous. They are adopted in almost every modern digital communication and storage system, such as wireless communications, optical communications, Flash memories, computer hard drives, sensor networks, and deep-space probing. New-generation and emerging applications demand codes with better error-correcting capability. On the other hand, the design and implementation of those high-gain error-correcting codes pose many challenges. They usually involve complex mathematical computations, and mapping them directly to hardware often leads to very high complexity.

VLSI Architectures for Modern Error-Correcting Codes serves as a bridge connecting advancements in coding theory to practical hardware implementations. Instead of focusing on circuit-level design techniques, the book highlights integrated algorithmic and architectural transformations that lead to great improvements on throughput, silicon area requirement, and/or power consumption in the hardware implementation.

The goal of this book is to provide a comprehensive and systematic review of available techniques and architectures, so that they can be easily followed by system and hardware designers to develop en/decoder implementations that meet error-correcting performance and cost requirements. This book can be also used as a reference for graduate-level courses on VLSI design and error-correcting coding. Particular emphases are placed on hard- and soft-decision Reed-Solomon (RS) and Bose-Chaudhuri-Hocquenghem (BCH) codes, and binary and non-binary low-density parity-check (LDPC) codes. These codes are among the best candidates for modern and emerging applications due to their good error-correcting performance and lower implementation complexity compared to other codes. To help explain the computations and en/decoder architectures, many examples and case studies are included.

More importantly, discussions are provided on the advantages and drawbacks of different implementation approaches and architectures.

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